Remarks

In the Office Action, the Examiner noted that claims 1-30, 34-39, and 45-50 are pending in the application, and that claims 1-30, 34-39, and 45-50 are rejected. Thus, claims 1-30, 34-39, and 45-50 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the arguments below.

In the Claims

Rejection Under 35 USC 103

The Examiner rejected claims 1, 2, 15-30, 34-39, 45, 48, and 50 under 35 U.S.C. § 103, as being anticipated by *Emma, et al.*, U.S. Patent No. 5,353,421 (hereinafter *Emma*) in view of *Forster et al*, U.S. Patent 4,181,942 (hereinafter *Forster*). Applicant respectfully traverses the rejection of claims 1, 2, 15-30, 34-39, 45, 48, and 50.

First, a brief discussion of *Forster* is helpful. Generally, *Forster* is directed to a microprocessor that has in its instruction set a branch instruction that may function as a conditional branch instruction or an unconditional branch instruction depending upon the value stored in a register of the microprocessor. The motivation for such an instruction is to save program space in a processor that has limited program instruction space such as *Forster*'s (1024 words of 12 bits each, see col. 3, lines 1-4). In particular, although *Forster* teaches a microprocessor that executes branch instructions, importantly, *Forster* does not teach a microprocessor that predicts branch instructions. That is, *Forster*'s microprocessor does not produce a target address of a branch instruction which is uncertain to be the correct target address. Rather, *Forster* teaches a branch instruction whose target address is included directly within the branch instruction, and there is no uncertainty about whether the target address is correct. That is, there is no subsequently produced correct target address which is compared with a predicted target address to determine whether the predicted target address is correct.

It is not surprising that *Forster* does not teach branch prediction since *Forster*'s microprocessor is a very old non-pipelined single chip microprocessor invented in the 1970s. As Applicant's Background section teaches at paragraphs 0006 to 0010, it is the

introduction of pipelining into microprocessors that created the need for branch prediction. However, *Forster* teaches a non-pipelined processor that executes a single instruction each cycle. See col.3, lines 11-12. Branch prediction is not needed, and is arguably not possible, in a non-pipelined processor, which explains why *Forster*'s processor does not include a branch predictor.

With respect to claim 1, the Examiner asserts that *Forster* teaches a branch predictor. Applicant respectfully asserts that *Forster* does not teach a branch predictor that provides a target address prediction of a branch instruction, as recited in claim 1. As explained above, *Forster* does not teach branch prediction, but merely teaches execution of a branch instruction. A target address prediction of a branch prediction, such as recited in claim 1, is an address that is not certain to be the target address of the branch instruction, as explained for example in paragraph 0096 of Applicant's specification. That is, microprocessors which perform branch prediction produce a correct target address subsequent to producing the predicted target address, and the possibility exists that the predicted target address provided by the branch predictors may not be the same as the subsequently produced correct target address, thus requiring correction of the prediction. See, for example, paragraph 0067 and paragraph 0158, last sentence. Because *Forster* does not teach a branch predictor that provides a target address prediction of a branch instruction, Applicant respectfully asserts that the Examiner has failed to make a *prima facie* case of obviousness with respect to claim 1 in citing *Emma* in view of *Forster*, and respectfully requests the Examiner to withdraw the rejection.

With respect to independent claims 28, 36, and 45, Applicant respectfully asserts that *Emma* in view of *Forster* does not obviate these claims for reasons similar to those discussed above with respect to claim 1, and requests the Examiner to withdraw the rejection.

Applicant respectfully asserts *Emma* in view of *Forster* does not obviate dependent claims 2-27, 29-30, 37-39, and 46-50 because they depend from independent claims 1, 28, 36, and 45, respectively, which are not obviated by *Emma* in view of *Forster* for the reasons discussed above.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

Respectfully submitted,

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"EXPRESS MAIL" mailing label number EO 004 339 417 US. Date of Deposit 3/28/05. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to the U.S. Commissioner of Patents and Trademarks, Alexandria, VA, 22313.

By: Alicia Nerwen